REMARKS

These remarks follow the order of the paragraphs of the office action. Relevant portions of the office action are shown indented and italicized.

DETAILED ACTION

2. Claims 1-5 and 10-14 are amended in response to the last office action. Osborne et al was cited in the last office action. Claims 1-21 are presented for examination.

Claim Rejections - 35 USC 5 112

3. The following is a quotation. of the first paragraph of 35 U.S.C. 112:
The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

4. Claims 1-21 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. Specification describes 'the first data processing system' of claim as a host system including CPUs and a memory and 'the second data processing system' of claim as a data communication interface such as a network adapter 60 [page 5, lines 6-10; pages, lines 10-12]; a 'descriptor table' is accessed by the first and second data processing systems. Specification further describes that there are a plurality of host computer systems and a plurality of attached devices [page 6, lines 4-81. However, Specification does not disclose that 'said first data processing system (accessing 'the descriptor table') comprises a plurality of host computer system': in other words, 'said descriptor table' is accessible by a single host computer system not accessible by a plurality of host systems. Specification also does not disclose that 'said second data processing system (accessing 'the descriptor table') comprises a plurality of attached devices.'

In response, the applicants respectfully state that indeed the intent of the specification includes embodiments wherein the descriptor table is accessible by a plurality of host systems. Specification also does indeed disclose embodiments wherein the second data processing system accessing the descriptor table comprises a plurality of attached devices.

The specification page 1, reads:

FIELD OF INVENTION

> The present invention relates to controlling flow of data, via a memory, between first and second data processing systems such as a host computer system and a data communications interface for communicating data between the host computer system and a data communications network.

Thus, it is the intent that the meaning of a host system is a system that has one or more hosts. This differentiates a system from a singular host which is referred to in the specification as 'a host' or 'the host'.

The specification page 1 continues to read:

BACKGROUND

> A conventional data processing network comprises **a plurality of host computer systems** and **a plurality of attached devices** all interconnected by an intervening network architecture such as an Ethernet architecture. The network architecture typically comprises one or more data communications switches. The **host computer systems** and the attached devices each form a node in the data processing network. Each host computer system typically comprises a plurality of central processing units and data storage memory device interconnected by a bus architecture such as a PCI bus architecture.

The present invention is to improve control of flow of data processing network in conventional data processing network which comprises a plurality of host computer systems.

Also, it shows that the specification does disclose that 'said second data processing system accessing 'the descriptor table comprises a plurality of attached devices.'

The specification page 2, reads:

SUMMARY OF THE INVENTION

> Thus, one aspect of the present invention, is to provide methods, apparatus and systems for controlling flow of data between first and second data processing systems via a memory. An example embodiment the apparatus comprising: a descriptor table for storing a plurality of descriptors for access by the first and second data processing systems; and, descriptor logic for generating the descriptors for storage in the descriptor table. The descriptors including a branch descriptor comprising a link to another descriptor in the table. The descriptor logic and descriptor table improve efficiency of data flow control between first and second data processing systems such as a host computer system and a data communications interface for communicating data between the host computer system and a data communications network.

Thus, this shows the intent of the invention to improve control of flow of first and second data processing systems. These processing systems may include a plurality of hosts.

Specification also does indeed disclose that 'said second data processing system which accesses 'the descriptor table' is shown to include embodiments wherein it comprises a plurality of attached devices.'

The specification page 3, reads:

> Viewing the present invention from another aspect, there is now provided a method for controlling flow of data between first and second data processing systems via a memory, the method comprising: storing in a descriptor table a plurality of descriptors for access by the first and second data processing systems; and, by descriptor logic, generating the descriptors for storage in the descriptor table, the descriptors including a branch descriptor comprising a link to another descriptor in the table.

Thus, the invention includes a plurality of descriptors for access by the first and second data processing systems, and a plurality of descriptor tables. These may represent tables from plurality of host computer systems.

The specification page 5, starting on line 2 reads:

> In an embodiment, the apparatus includes: a descriptor table for storing a plurality of descriptors for access by the first and second data processing systems; and descriptor logic for generating the descriptors for storage in the descriptor table, the descriptors including a branch descriptor comprising a link to another descriptor in the table.

A plurality of descriptors are stored in each of the plurality of descriptor tables.

The specification page 6, starting on line 4 reads:

> Referring first to Figure 1, an example of a data processing network embodying the present invention comprises **a plurality of host computer systems** 10 and **a plurality of attached devices** 20 interconnected by an intervening network architecture 30 such as an InfiniBand network architecture (InfiniBand is a trade mark of the InfiniBand Trade Association). ... ... Each host computer system 10 comprises a plurality of central processing units (CPUs) 50, and a memory 60 interconnected by a bus architecture 70 such as a PCI bus architecture.

Thus, the present invention for controlling flow of data between first and second data processing systems has embodiments where a data processing system comprises a plurality of host computer systems and a plurality of attached devices. The paragraph also refers to each host computer system, from the plurality of host computer systems. Thus, these devices indeed make up the a second data processing system which access the descriptor table in accordance with the specification description.

Thus, it is apparent the specification of the present invention indeed by intent and in words teaches and discloses that 'said first data processing system (accessing 'the descriptor table') comprises a plurality of host computer system. Embodiments are included wherein 'said descriptor table' **is accessible** by either a single host computer system or by a plurality of host

systems. So it is apparent that the specification also does indeed disclose that 'said second data processing system (accessing 'the descriptor table') comprises a plurality of attached devices.'

Examiner is respectfully requested to give patentable weight to both limitations, namely:

'said first data processing system accessing 'the descriptor table comprises a plurality of host computer systems, such that 'said descriptor table' is accessible by a plurality of host systems, and to

'said second data processing system (accessing 'the descriptor table') comprises a plurality of attached devices.'

These will certainly contribute to the non-disclosed limitations in the present claims, and bring the present claims to allowance.

Claim Rejections -35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill In the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 1, 2,6-11, and 14-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Osborne et al. (US 5,751,951] in view of Benner [US 5,961,659].

In response, the applicants respectfully state that exception is taken with the combination of Benner with Osborne Claims 1, 2,6-11, and 14-21 provide flow control of data between a memory of a host computer system and a data communications interface for communicating data between the host computer system and a data communications network. It was shown that Osborne fails to teach or anticipate these claims. This is so even when combined with Benner.

The art cited to Benner is entitled, "Independent simultaneous queueing of message descriptors." The Benner abstract reads:

> "Two independent pointers within a message descriptor are used to link the message descriptor to various queues during transmission of a message from a sender node to a receiver node within a computer environment. In particular, one pointer is used to link the message descriptor on either a pending send queue or a send queue, while the other pointer is used to link the message descriptor on either an unacknowledged queue or an acknowledged queue. For example, when a message is sent, it is removed from the send queue using one pointer and placed on the unacknowledged queue using the other pointer. Further, if the message is resent, it is linked back onto the send queue using the send queue pointer without disturbing the order of the message on the unacknowledged queue. Thus, ordering of message transmission is preserved, even when a message is sent multiple times."

Thus, even though Benner is concerned with descriptor, Benner is primarily concerned with using two independent pointers within a message descriptor are used to link the message descriptor to various queues during transmission of a message from a sender node to a receiver node within a computer environment. This is not a teaching of or related to controlling flow of data between a memory of a host computer system and a data communications interface for communicating data between the host computer system and a data communications network, even if both employ descriptors.

Besides, there is no reason to combine Osborne concerned with a "non-blocking transmit interface that incorporates optimized buffer modes, dynamic and static chaining, streaming and the utilization of small packet formats, with Benner concerned with using two independent pointers within a message descriptor are used to link the message descriptor to various queues during transmission of a message from a sender node to a receiver node within a computer environment. This is using hindsight in an attempt to find a combination that allegedly teaches or make obvious Claims 1, 2,6-11, and 14-21. This is not allowed, especially when apparently neither reference alludes to the other. Thus Claims 1, 2,6-11, and 14-21 are allowable over the combined art.

> *As for claim 1, Osborne et al teach an apparatus comprising: a descriptor table [e.g., "ring queue" in col. 1, line 59-col. 2, line 10; col. 5, lines 53-64; col. 14, lines 21-35], said apparatus for controlling [col. 14, lines 20-35] flow of data between first [e.g.1 "host" in fig. 3A, "computers" in col. 1, lines 20-25 and relevant description] and second data processing systems [e.g., "network interface card" in fig. 3A and relevant description] via a memory, said descriptor table for storing a plurality of descriptors for access [col 1, lines 59-64; col. 2, lines 15-21; col. 16, lines 6-24] by the first and second data processing systems, said first processing system comprises a plurality of host computer systems ["computers" in col. 1, lines 20-25], said second data processing*

comprising a plurality of attached devices [other networked computers and data systems" in col. 1, lines 20-25interconnected by an intervening network architecture, said network architecture comprises a plurality of data communications switches ["network switches" in col. 1, lines 13-20], said host computer system and attached devices each forming a node ["node"in col, 1, lines 13-20] in a data processing network, each host computer system comprises a memory interconnected by a PCI bus architecture ["PCI bus 152" in fig. 3A];

a network adapter ["network interface card" in fig. 3A and relevant description] also connected to the bus architecture for communicating data between the host computer system and other nodes in the data processing network via the network architecture [col. 1, lines 13-30]; and

descriptor logic for generating [inserting into the queue using formats shown in figs. 3B-14 and relevant description; col. 2, lines 15-17; col. 15, lines 1-7; cal. 19, lines 46-47] the descriptors for storage in the descriptor table, the descriptors including a branch descriptor comprising a link [e.g., fig. 2A, 2B and relevant description] to another descriptor in the table.

However, Osborne et al do not expressly disclose that the host computer system comprises a plurality of central processing units. Benner teaches an apparatus for controlling flow of data between first and second processing systems via a memory having a descriptor table [fig. 3B] wherein the first processing systems comprises a plurality of host computer systems [nodes 104 in fig. 1], each host computer system comprises a plurality of central processing units [microprocessors 106 in fig. 1] and a memory [main memory 108], and the second processing systems comprises a plurality of attached devices interconnected by an intervening network architecture [fig. 1].

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Osborne et al and Benner because they both teach an apparatus for controlling flow of data between first and second processing systems via a memory having a descriptor table and Benner's teaching of multiple central processing units included in each host computer system of the first processing system would increase efficiency in processing [Benner: col. 4, lines 5-9] of the host computer of Osborne et al.

In response, the applicants respectfully state that it was shown that indeed Osborne fails to teach the

elements of Claims 1, 2,6-11, and 14-21. A review of Benner fails to show any teaching by Benner of an apparatus for controlling flow of data between first and second processing systems via a memory having a descriptor table, in Fig. 3B or elsewhere. Benner certainly doesn't allude to any first processing systems comprising **a plurality of host computer systems** in nodes 104 in fig. 1 or elsewhere. Benner certainly doesn't allude to any host computer system that comprises a plurality of central processing units in microprocessors 106 in fig. 1, or elsewhere. Benner

certainly doesn't allude to any memory, and a second processing systems comprises a plurality of attached devices interconnected by an intervening network architecture in [fig. 1, or elsewhere as in Claims 1, 2,6-11, and 14-21. Thus Claims 1, 2,6-11, and 14-21. are allowable over the combined art.

7. As for claim 2, Osborne et al teach the combination of Osborne et al and Benner teaches the network adapter comprises a pluggable option card [implicit to the PCI bus 'network interface 'card"] having a connector such as an edge connector for removable insertion into the bus architecture of the host computer system, said option card carrying:

an Integrated System on a Chip [NIC chip 154 in fig. 3A] connected to the bus architecture via a connector, at least one third level memory modules [local memory 165 in fig. 3A1 connected to the chip, and an interposer [UTOPIA 156, 158 in fig. 3A1 connected to the chip for communicating data between media of network architecture and the chip, said interposer providing a physical connection to the network, and wherein the descriptors generated by the descriptor logic comprising a frame descriptor defining a data packet to be communicated between a location in the memory and the second data processing system, and a pointer descriptor identifying the location in the memory [e.g., figs. 2A-14 and relevant description; col. 5, lines 53-64].

8. As for claim 6, Osborne et al teach the descriptor table comprising a cyclic descriptor list [col. 1, lines 61-64].

9. As for claim 7, Osborne et al teach the first data processing system comprising a host computer system [host in fig. 3A and relevant description].

10. As for claim 8, Osborne et al teach the second data processing system comprising a data communications interface for communicating data between a host computer system and a data communications network [host and network interface card in fig. 3A and relevant description].

11. As for claim 9, Osborne et al teach a host computer system having a memory, a data communications interface for communicating data between the host computer system and a data communications network for controlling flow of data between the memory of the host computer system and the data communications interface [fig. 3A and relevant description].

12. As for claim 10, Osborne et al teach a method comprising controlling flow of data between first and second data processing systems via a memory, the steps of controlling

comprising: storing [e.g., figs. 2A-2C and relevant description] in a descriptor table a plurality of descriptors for access [col. 3, lines 28–42] by the first and second data processing systems,

forming said first processing system to comprise a plurality of host computer systems ["computer? in col. 1, lines 20-25], said second data processing to comprise a plurality of attached devices ["other networked computers and data systems" in col. 1, lines 20-25 interconnected by an intervening network architecture, said network architecture comprises a plurality of data communications switches ["network switches" in col. 1, lines 13-20], said host computer system and attached devices each forming a node ["node" in col. 1, lines 13-20] in a data processing network, each host computer system comprises a memory interconnected by a PCI bus architecture ["PCI bus 152" in fig. 3A] including a network adapter ["network interface card" in fig: 3A and relevant description] also connected to the bus architectUre for communicating data between the host computer system and other nodes in the data processing network via the network architecture [col. 1, lines 13-30]; and

by descriptor logic, generating [e.g., col. 19, lines 46-47] the descriptors for storage in the descriptor table, the descriptors including a branch descriptor comprising a link [e.g., fig. 2A and relevant description] to another descriptor in the table.

However, Osborne et al do not expressly disclose that the host computer system comprises a plurality of central processing units. Benner teaches an apparatus for controlling flow of data between first and second processing systems via a memory having a descriptor table [fig. 3B] wherein the first processing systems comprises a plurality of host computer systems [nodes 104 in fig. 1], each host computer system comprises a plurality of central processing units [microprocessors 106 in fig. 1] and a memory [main memory 108], and the second processing systems comprises a plurality of attached devices interconnected by an intervening network architecture [fig. 1].

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Osborne et al and Benner because they both teach an apparatus for controlling flow of data between first and second processing systems via a memory having a descriptor table and Benner's teaching of multiple central processing units included in each host computer system of the first processing system would increase efficiency in processing [Benner: col. 4, lines 5-9] of the host computer of Osborne et al.

13. As for claim 14, Osborne et al teach the descriptor table comprising a plurality of descriptors lists sequentially linked together via branch descriptors therein [e.g., figs. 2A- 2C and relevant description], wherein a branch descriptor comprises description of the descriptor location being link lists of descriptors, using information in the descriptors for control by software in the host of data movement operations performed by TX and RX

LCP engines [IX 155, RX 157 in fig. 3A], using the information to process a frame to generate a IX packet header in the header of the frame ['frame descriptor in col. 5, lines 53-65].

14. As for claims 11 and 15-21, Osborne et al teach the claimed limitations as discussed above.

In response, the applicants respectfully state *that exception is taken with the alleged teachings of the elements of* Claims 1, 2,6-11, and 14-21 in Osborne with or without Benner. Thus Claims 1, 2,6-11, and 14-21 *are allowable over the combined art.*

Allowable Subject Matter

15. Claims 3-5, 12, and 13 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims and amended to overcome the rejections under 35 U.S.C. 112, first paragraph, set forth in this office action.

In response, the applicants respectfully state that in order to bring the allowable claims to allowance, claim 1 is amended to include the limitation of claims 2 and 3, and claim 11 is amended to include the limitation of claims 12. This is done without submitting to the arguments of the office action.

Applicants have amended claim 1 and 11 and canceled claims 2, 3, and 12. from further consideration in this application. Applicants are not conceding in this application that those claims are not patentable over the art cited by the Examiner, as the present claim amendments and cancellations are only for facilitating expeditious prosecution of the allowable subject matter noted by the examiner. Applicants respectfully reserve the right to pursue these and other claims in one or more continuations and/or divisional patent applications."

It is anticipated that this amendment brings this application in order for a Notice of Allowance. If any questions remain, please contact the undersigned representative.

Please charge any fee necessary to enter this paper to deposit account 50-0510.

Respectfully submitted,

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